Preliminary Data Sheet, Rev. 3
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Lucent Technologies
Bell Labs Innovations

UNIVERSAL SERIAL BUS

USS-720 *Instant USB*™ USB-to-*IEEE** 1284 Bridge

Features

Device Features:

- Full compliance with the *Universal Serial Bus Specification Revision 1.0*
- On-chip transceivers for USB
- Low power consumption allows part to be powered from USB connection
- Dual on-chip USB packet buffers for fast response
- Fully compatible USB host device drivers available
- Fully compliant with USB printer device class specification
- Implemented in Lucent Technologies Microelectronics Group's 0.35 µm, 3 V standard-cell library
- Complete single-chip solution in a 44-pin MQFP
- Evaluation kit available

IEEE 1284 (Parallel) Features:

- Transparent, fully automatic support for true bidirectional communication
- Hardware initiates and manages automatic negotiation for the fastest protocol available
- Supports standard PC parallel port register-based operation
- Support of multiple logical channels
- Maximum throughput: 1.216 Mbytes/s (ECP mode)

Description

The USS-720 integrated circuit connects an *IEEE* 1284 parallel port peripheral to the universal serial bus (USB). It is designed to be a low-cost, single-chip embedded solution requiring minimal external components. It is suitable for a wide range of applications, from integrated applications where the IC is mounted on a printed-circuit board inside a product, to stand-alone applications where the chip provides a standard parallel port to a USB-capable computer. The USS-720 software included in the Evaluation Kit allows peripheral vendors to evaluate and test the USS-720 device, which is embedded in the *Centronics*† end of a USB-to-parallel port cable provided with the kit. This solution requires no firmware changes on the parallel port peripheral.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
† *Centronics* is aregistered trademark of Centronics Data Computer Corporation.

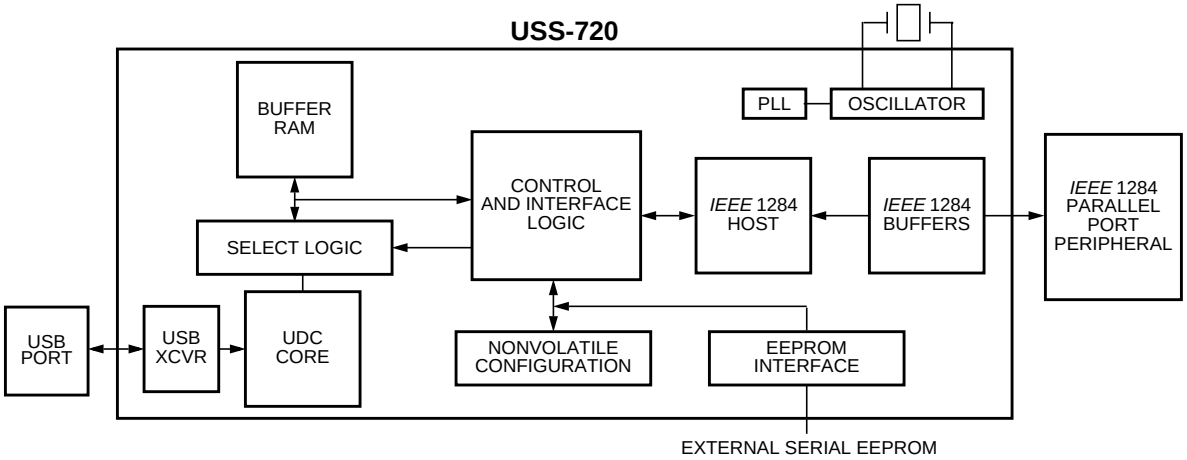

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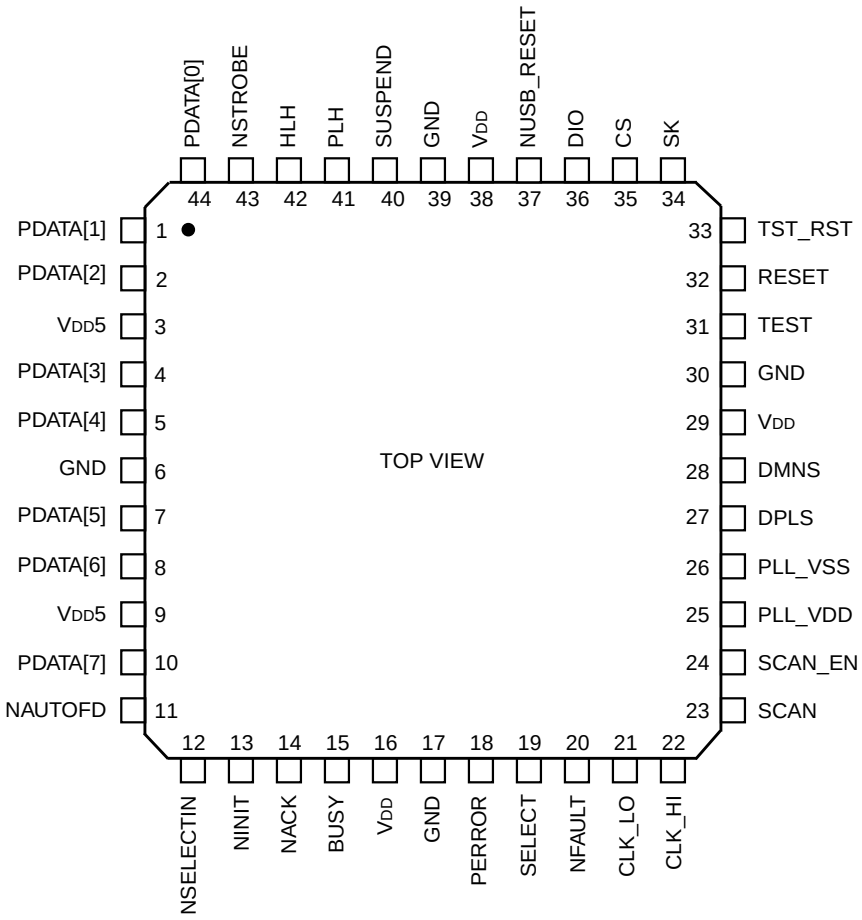
Figure 1. Block Diagram

Note: Advisories are issued as needed to update product information. When using this data sheet for design purposes, please contact your Lucent Technologies Microelectronics Group Account Manager to obtain the latest advisory on this product.

Table of Contents

Pin Information



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Note: An N before symbol names indicates active-low.

Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Symbol*	Type	Name/Description
1	PDATA[1]	I/O	**Parallel Port Data Signal Bit 1.**
2	PDATA[2]	I/O	**Parallel Port Data Signal Bit 2.**
3	VDD5	P	**5 V Power Supply for 5 V Parallel Port Signals.**
4	PDATA[3]	I/O	**Parallel Port Data Signal Bit 3.**
5	PDATA[4]	I/O	**Parallel Port Data Signal Bit 4.**
6	GND	P	**Ground.**
7	PDATA[5]	I/O	**Parallel Port Data Signal Bit 5.**
8	PDATA[6]	I/O	**Parallel Port Data Signal Bit 6.**

* An N before symbol names indicates active-low.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol*	Type	Name/Description
9	$V_{DD}5$	P	**5 V Power Supply for 5 V Parallel Port Signals.**
10	PDATA[7]	I/O	**Parallel Port Data Signal Bit 7.**
11	NAUTOFD	O	**Parallel Port nAutoFd Signal (Active-Low).**
12	NSELECTIN	O	**Parallel Port nSelectIn Signal (Active-Low).**
13	NINIT	O	**Parallel Port nInit Signal (Active-Low).**
14	NACK	I	**Parallel Port nAck Signal (Active-Low).**
15	BUSY	I	**Parallel Port Busy Signal.**
16	V_{DD}	P	**3.3 V Power Supply.**
17	GND	P	**Ground.**
18	PERROR	I	**Parallel Port PError Signal.**
19	SELECT	I	**Parallel Port Select Signal.**
20	NFAULT	I	**Parallel Port nFault Signal (Active-Low).**
21	CLK_LO	I	**Clock Low.** Crystal or CMOS input.
22	CLK_HI	O	**Clock High.** Crystal or no connection.
23	SCAN	I	**Scan.** This signal is only used for production testing. Tie to GND for normal operation.
24	SCAN_EN	I	**Scan Enable.** When high, internal chip scan is enabled. This signal is only used for production testing. Tie to GND for normal operation.
25	PLL_VDD	P	**3.3 V Analog Power Supply for PLL.**
26	PLL_VSS	P	**Analog Ground for PLL.**
27	DPLS	I/O	**USB DPLS Signal.**
28	DMNS	I/O	**USB DMNS Signal.**
29	V_{DD}	P	**3.3 V Power Supply.**
30	GND	P	**Ground.**
31	TEST	I	**Test.** This signal is only used for production testing. Tie to GND for normal operation.
32	RESET	I	**Reset.** This signal is only used for production testing. Tie to GND for normal operation.
33	TST_RST	I	**Test Reset.** This signal is only used for production testing. Tie to GND for normal operation.
34	SK	O	**Serial ROM Clock.**
35	CS	O	**Serial ROM Chip Select.**
36	DIO	I/O	**Serial ROM Data Signal.**
37	NUSB_RESET	O	**USB Reset (Active-Low).** Indicates USB reset condition.
38	V_{DD}	P	**3.3 V Power Supply.**
39	GND	P	**Ground.**
40	SUSPEND	O	**Suspend.** Indicates USB bus in suspend.
41	PLH	I	**Parallel Port Peripheral Logic High Signal.**
42	HLH	O	**Parallel Port Host Logic High Signal.**
43	NSTROBE	O	**Parallel Port nStrobe Signal (Active-Low).**
44	PDATA[0]	I/O	**Parallel Port Data Signal.**

* An N before symbol names indicates active-low.

Overview

The USS-720 creates a bridge between one USB port and one *IEEE* 1284 enhanced parallel port. Internally, the USS-720 contains an integrated USB transceiver, a USB device controller (UDC) core, an *IEEE* 1284 core, integrated *IEEE* 1284 buffers, storage for USB configuration data, data buffers, and control logic to tie the blocks together. The USS-720 also contains an onboard oscillator, PLL, and reset block for single-chip operation.

In use, the USB port of the USS-720 is connected via a USB cable to a host computer or the downstream port of a USB hub. Host software sends commands and data to the USS-720 and receives status and data from the USS-720 using the USB protocol.

The *IEEE* 1284 enhanced parallel port of the device is connected to a peripheral device. If the peripheral is *IEEE* 1284 compatible, then the associated features and communication modes can be used. The USS-720 provides both automatic and manual operation of the *IEEE* 1284 port.

USB Port

The USB port on the USS-720 is electrically and logically compliant with the *USB Specification Revision 1.0*.

Device Descriptor, Configurations, and Interfaces

Supported Descriptors

- **Device**.
- **Configuration**.
- **Interface**. The USS-720 device supports one interface with three alternate settings.
  - — Interface 0, alternate settings 0 and 1 are compliant with the *USB Device Class Definition for Printing Devices, Release Candidate 1.0*.
  - — Interface 0, alternate setting 2 is a vendor-specific interface.
- **Endpoint**. The USS-720 supports the following endpoints:
  - — Control endpoint. Accessible as endpoint 0 in all three alternate interface settings.
  - — Bulk Out endpoint. Accessible as endpoint 1 in all three alternate interface settings.
  - — Bulk In endpoint. Accessible as endpoint 2 in alternate interface settings 1 and 2.
  - — Interrupt endpoint. Accessible as endpoint 3 in alternate interface setting 2.
- **String**.

Descriptor Locations

Descriptor data is supplied from an external ROM or other device. The USS-720 provides support for 93CS56 and 93CS66 EEPROM interfaces. (**Note:** Substitution EEPROM components must be pin and functional compatible with the 93CS56L/66L. 93C56L/66L, 93CS46L, and 93C46L EEPROM parts will **not** function correctly with the USS-720.) The format for the externally supplied descriptor data requires that the descriptors loaded be preceded by the total length of the descriptor to be returned. In the case of the device descriptor, this value would be 0x12, which is redundant since the descriptor returned is always 0x12 bytes long; the first byte of the descriptor would also be 0x12. The length of the configuration descriptor, however, is not the same as the first byte of that descriptor, since the configuration descriptor and all associated interface and endpoint descriptors are returned as a whole.

The USS-720 also contains a set of device, configuration, interface, and endpoint descriptors that may be used in development and prototyping. Retrieval of the onboard descriptors will occur if no external descriptor data is supplied.

USB Port (continued)

The format for the externally supplied data is as shown in Table 2. The addressing for the specified EEPROM device is word aligned, so the following restrictions are placed upon the starting locations for the configuration and string descriptors.

- The configuration descriptor must start at word address 0x13 (byte address 0x26).
- String descriptors must start at an address that is aligned on a double-word boundary.

Table 2. Externally Supplied Data Format

Byte Address	Word Address	Value
0x00	0x00	0x12
0x01—0x12	—	Device descriptor as defined in *USB Specification Revision 1.0*.
0x26	0x13	Total length of string to be returned in response to a GET_CONFIGURATION_DESCRIPTOR request.
0x27—0x2F	—	Configuration descriptor as defined in *USB Specification Revision 1.0*.
0x30—???*	—	Interface and endpoint descriptors to be returned in response to a GET_CONFIGURATION_DESCRIPTOR request.
Any even word address beyond the end of the configuration descriptor return string.		Length of string to return in response to a GET_STRING_DESCRIPTOR request. This address divided by two should be included in the low byte of the wIndex field of the GET_DESCRIPTOR standard command.
Next address—end of string descriptor.		String descriptor as defined in *USB Specification Revision 1.0*.

* The question marks (???) indicate that this byte address value is determined for the user's application based on the above information. The number is going to vary depending on how the user formats their configuration information.

Note: Tables 3—14 describe the descriptor data contained in the USS-720's internal ROM. This information can be used as a guide in creating the externally supplied descriptor data.

Onboard Device Descriptor

There is only one device descriptor for each USB device. This descriptor contains the definitions of the device class and the device subclass, among other things.

Table 3. Device Descriptor

Offset	Field	Size	Value	Description
0	bLength	Byte	0x12	Size of this descriptor in bytes.
1	bDescriptorType	Byte	0x01	Device descriptor type.
2	bcdUSB	Word	0x0100	USB Specification release number in BCD.
4	bDeviceClass	Byte	0x00	Interface specific. See Tables 6, 8, and 11.
5	bDeviceSubClass	Byte	0x00	Interface specific. See Tables 6, 8, and 11.
6	bDeviceProtocol	Byte	0x00	Interface specific. See Tables 6, 8, and 11.
7	wMaxPacketSize0	Byte	0x08	Maximum packet size for endpoint 0.
8	idVendor	Word	0x047E	Vendor ID for Lucent Technologies.
10	idProduct	Word	0x1001	Product ID.
12	bcdDevice	Word	0x0103	Device release number in BCD.
14	iManufacturer	Byte	0x00	Index of string descriptor describing manufacturer.
15	iProduct	Byte	0x00	Index of string descriptor describing this product.
16	iSerialNumber	Byte	0x00	Index of string descriptor describing the device's serial number.
17	bNumConfigurations	Byte	0x01	Number of possible configurations.

USB Port (continued)

Configuration Descriptor

The USS-720 has one default configuration descriptor. This descriptor has one interface, which has three alternate settings. The three alternate settings and the endpoints that they support are shown in Table 4.

Table 4. Alternate Settings and Supported Endpoints

Endpoint	Interface		
	Alternate Setting 0	**Alternate Setting 1**	**Alternate Setting 2**
Control Pipe	Endpoint Number 0 8 bytes	Endpoint Number 0 8 bytes	Endpoint Number 0 8 bytes
Bulk Out Pipe	Endpoint Number 1 64 bytes	Endpoint Number 1 64 bytes	Endpoint Number 1 64 bytes
Bulk In Pipe	—	Endpoint Number 2 64 bytes	Endpoint Number 2 64 bytes
Interrupt Pipe	—	—	Endpoint Number 3 4 bytes

Table 5. Configuration Descriptor

Offset	Field	Size	Value	Description
0	bLength	Byte	0x09	Size of this descriptor in bytes.
1	bDescriptorType	Byte	0x02	Configuration descriptor type.
2	bTotalLength	Word	0x004E	Number of bytes in this configuration. This includes the configuration descriptor plus all of the interface and endpoint descriptors.
4	bNumInterfaces	Byte	0x01	The USS-720 has one interface.
5	bConfigurationValue	Byte	0x01	Value to use as an argument to Set Configuration to select this configuration.
6	iConfiguration	Byte	0x00	Index of string descriptor describing this configuration.
7	bmAttributes	Byte	0x80	Configuration characteristics: **Bit** **Description** **USS-720** 7 Bus-powered. Set. 6 Self-powered. Cleared. 5 Remote wakeup. Cleared. 4—0 Reserved, set to 0. Cleared.
8	MaxPower	Byte	0x31	Maximum power consumption of this configuration. Units are mA * 2; therefore, the value 0x31 is equivalent to 98 mA.

USB Port (continued)

Interface Descriptors

The USS-720 supports a single interface with three alternate settings.

Interface 0, Alternate Setting 0 (I0:A0)

Table 6. Interface Descriptor, I0:A0

Offset	Field	Size	Value	Description
0	bLength	Byte	0x09	Size of this descriptor in bytes.
1	bDescriptorType	Byte	0x04	Interface descriptor type.
2	bInterfaceNumber	Byte	0x00	Zero-based value identifying the number of this interface.
3	bAlternateSetting	Byte	0x00	Value used to select this alternate interface.
4	bNumEndpoints	Byte	0x01	Number of endpoints used by this descriptor.
5	bInterfaceClass	Byte	0x07	Printer class.
6	iInterfaceSubClass	Byte	0x01	Printer subclass.
7	bInterfaceProtocol	Byte	0x01	Unidirectional interface.
8	iInterface	Byte	0x00	Index to string describing this interface.

Table 7. Bulk Out Endpoint Descriptor, I0:A0:E1

Offset	Field	Size	Value	Description
0	bLength	Byte	0x07	Size of this descriptor in bytes.
1	bDescriptorType	Byte	0x05	Endpoint descriptor type.
2	bEndpointAddress	Byte	0x01	This is an Out endpoint, endpoint number 1.
3	bmAttributes	Byte	0x02	This is a Bulk endpoint.
4	wMaxPacketSize	Word	0x0040	Maximum data transfer size.
6	bInterval	Byte	0x00	Does not apply to bulk endpoints.

USB Port (continued)

Interface 0, Alternate Setting 1 (I0:A1)

Table 8. Interface Descriptor, I0:A1

Offset	Field	Size	Value	Description
0	bLength	Byte	0x09	Size of this descriptor in bytes.
1	bDescriptorType	Byte	0x04	Interface descriptor type.
2	bInterfaceNumber	Byte	0x00	Zero-based value identifying the number of this interface.
3	bAlternateSetting	Byte	0x01	Value used to select this alternate interface.
4	bNumEndpoints	Byte	0x02	Number of endpoints used by this descriptor.
5	bInterfaceClass	Byte	0x07	Printer class.
6	iInterfaceSubClass	Byte	0x01	Printer subclass.
7	bInterfaceProtocol	Byte	0x02	Bidirectional interface.
8	iInterface	Byte	0x00	Index to string describing this interface.

Table 9. Bulk Out Endpoint Descriptor, I0:A1:E1

Offset	Field	Size	Value	Description
0	bLength	Byte	0x07	Size of this descriptor in bytes.
1	bDescriptorType	Byte	0x05	Endpoint descriptor type.
2	bEndpointAddress	Byte	0x01	This is an Out endpoint, endpoint number 1.
3	bmAttributes	Byte	0x02	This is a Bulk endpoint.
4	wMaxPacketSize	Word	0x0040	Maximum data transfer size.
6	bInterval	Byte	0x00	Does not apply to Bulk endpoints.

Table 10. Bulk In Endpoint Descriptor, I0:A1:E2

Offset	Field	Size	Value	Description
0	bLength	Byte	0x07	Size of this descriptor in bytes.
1	bDescriptorType	Byte	0x05	Endpoint descriptor type.
2	bEndpointAddress	Byte	0x82	This is an In endpoint, endpoint number 2.
3	bmAttributes	Byte	0x02	This is a Bulk endpoint.
4	wMaxPacketSize	Word	0x0040	Maximum data transfer size.
6	bInterval	Byte	0x00	Does not apply to Bulk endpoints.

USB Port (continued)

Interface 0, Alternate Setting 2 (I0:A2)

Table 11. Interface Descriptor, I0:A2

Offset	Field	Size	Value	Description
0	bLength	Byte	0x09	Size of this descriptor in bytes.
1	bDescriptorType	Byte	0x04	Interface descriptor type.
2	bInterfaceNumber	Byte	0x00	Zero-based value identifying the number of this interface.
3	bAlternateSetting	Byte	0x02	Value used to select this alternate interface.
4	bNumEndpoints	Byte	0x03	Number of endpoints used by this descriptor.
5	bInterfaceClass	Byte	0xFF	Vendor specific.
6	iInterfaceSubClass	Byte	0x00	—
7	bInterfaceProtocol	Byte	0xFF	Vendor specific.
8	iInterface	Byte	0x00	Index to string describing this interface.

Table 12. Bulk Out Endpoint Descriptor, I0:A2:E1

Offset	Field	Size	Value	Description
0	bLength	Byte	0x07	Size of this descriptor in bytes.
1	bDescriptorType	Byte	0x05	Endpoint descriptor type.
2	bEndpointAddress	Byte	0x01	This is an Out endpoint, endpoint number 1.
3	bmAttributes	Byte	0x02	This is a Bulk endpoint.
4	wMaxPacketSize	Word	0x0040	Maximum data transfer size.
6	bInterval	Byte	0x00	Does not apply to Bulk endpoints.

Table 13. Bulk In Endpoint Descriptor, I0:A2:E2

Offset	Field	Size	Value	Description
0	bLength	Byte	0x07	Size of this descriptor in bytes.
1	bDescriptorType	Byte	0x05	Endpoint descriptor type.
2	bEndpointAddress	Byte	0x82	This is an In endpoint, endpoint number 2.
3	bmAttributes	Byte	0x02	This is a Bulk endpoint.
4	wMaxPacketSize	Word	0x0040	Maximum data transfer size.
6	bInterval	Byte	0x00	Does not apply to Bulk endpoints.

Table 14. Interrupt Endpoint Descriptor, I0:A2:E3

Offset	Field	Size	Value	Description
0	bLength	Byte	0x07	Size of this descriptor in bytes.
1	bDescriptorType	Byte	0x05	Endpoint descriptor type.
2	bEndpointAddress	Byte	0x83	This is an In endpoint, endpoint number 3.
3	bmAttributes	Byte	0x03	This is an Interrupt endpoint.
4	wMaxPacketSize	Word	0x0004	Maximum data transfer size.
6	bInterval	Byte	0x01	This pipe should be serviced every frame.

USB Port (continued)

Pipes

Four pipes are defined: Control, Bulk Out, Bulk In, and Interrupt.

Control Pipe

The Control pipe is the default pipe, used for USB setup and control packets. Its maximum packet size is 8 bytes. The Control pipe is also used for class- and vendor-specific commands that:

- Configure class- and vendor-specific features.
- Retrieve Device, Configuration, and String descriptors.

Note: Descriptor data shares the physical buffer used to transfer Bulk In data. Retrieving this data will result in the loss of any reverse channel data currently in the Bulk In buffer.

- Read and write the parallel port registers.
  - — Access standard parallel port register set.
  - — Read/write an address byte from/to the peripheral in EPP Mode.
  - — Read/write a data byte from/to the peripheral in EPP Mode (but multiple bytes can be transferred more efficiently via the Bulk Out pipe).
- Read Printer Class Get Device ID data.

Note: This data shares the physical buffer used to transfer Bulk In data. Retrieving this data will result in the loss of any reverse channel data currently in the Bulk In buffer.

Bulk In Pipe

The Bulk In pipe is used to read data bytes from the peripheral in Automatic Mode and register-based ECP Mode. Its maximum packet size is 64 bytes. The buffer used for this pipe is shared with the Control pipe for descriptor data and *IEEE* 1284 Device ID string data. The Control pipe has priority over Bulk In data, so any data in this buffer when a request is made for descriptor data or *IEEE* 1284 Device ID string will be lost.

Bulk Out Pipe

The Bulk Out pipe is used to send data to the peripheral in Automatic Mode and in Compatibility, EPP, or ECP Register Modes. Its maximum packet size is 64 bytes.

Interrupt Pipe

The Interrupt pipe is used to report changes in parallel port and buffer status to the host. Interrupt packets are 4 bytes in length. When the Interrupt pipe is enabled by host software, the host automatically polls the USS-720 once per frame. The USS-720 returns 4 bytes of status whenever an interrupt condition exists, as described in the Interrupts section on page 23, and returns nothing otherwise. This enables the host to detect and react to parallel port and buffer status changes without explicit polling.

Interpipe Synchronization

With commands and data going to different pipes, and data potentially being buffered inside the USS-720, it could be difficult for host software to maintain serialization of operations on the peripheral. This can be done by reading the registers to determine the status of the USS-720. Or, the Interrupt pipe status mechanism described above can be used to alleviate this problem. Software can use the port status and buffer status information thus returned to determine when buffered data has been sent and when port control commands have been processed and it is safe to continue. Since interrupt information is returned to the software automatically and only when it changes, overhead for the host operating system and driver software is kept low when using the interrupt pipe as opposed to polling the registers.

Requests

The USS-720 can respond to three different types of requests:

- Standard USB device requests.
- Class-specific requests.
- Vendor-specific requests.

Standard Requests

The USS-720 supports all of the standard device requests described in Chapter 9, Device Framework, of the USB Specification except Set Descriptor:

- Clear Feature.
- Get Configuration.
- Get Descriptor. Direct requests for interface and endpoint descriptors are not supported in the USS-720 and will cause the Control pipe to be stalled.
- Get Interface.
- Get Status.
- Set Address.
- Set Configuration.
- Set Interface.
- Set Feature.

USB Port (continued)

Printer Class-Specific Requests

Printer class-specific requests supported by the USS-720 are listed in Table 15.

Table 15. Class-Specific Requests

Label	bmRequestType	bRequest	wValue	wIndex	wLength	Data
GET_DEVICE_ID	10100001B	0	Config Index	Interface and Alternate Setting	Maximum Length	*IEEE* 1284 Device ID String
GET_PORT_STATUS	10100001B	1	Zero	Interface	1	BYTE
SOFT_RESET	00100011B	2	Zero	Interface	Zero	[None]

GET_DEVICE_ID

This request returns an *IEEE* 1284 Device ID string. This command is supported by all three alternate interface settings.

The Device ID is a length field followed by a case-sensitive string of ASCII characters. The first 2 bytes are the length of the sequence, including the two length bytes. The first byte is the most significant; length values of 0000h, 0001h, and 0002h are reserved.

Following the two length bytes, the sequence is composed of a series of keys and values of the form:

key: value {, value};

repeated for each key. As indicated, each key will have one value, and may have more than one value. The minimum necessary keys are MANUFACTURER, COMMAND SET, and MODEL (case sensitive). These keys may be abbreviated as MFG, CMD, and MDL. Each key (and each value) is a string of characters. Any characters except colon (:), comma (,), and semicolon (;) may be included as part of the key or value string. Any leading or trailing white space in the string is ignored by the parsing program, but is still counted as part of the overall length of the sequence.

For more details, see *IEEE* 1284-1994, Section 7.6.

Note: The USS-720 satisfies this request by requesting Device ID data from the attached *IEEE* 1284 peripheral. If the peripheral does not support Device ID, the USS-720 will return a zero-length data packet to the host.

GET_PORT_STATUS

This request returns the current status of the printer. Table 16 defines the data returned and describes the format of the status data. This command is only supported by the two printer class-specific alternate interface settings (0 and 1). Attempts to issue this command to interface 0, alternate setting 2 will result in a stall.

Table 16. Get Port Status Data

Bit	Description
7—6	Reserved, will always read 0.
5	Paper error.
4	Select.
3	Not error: 0 = error, 1 = no error.
2—0	Reserved, will always read 0.

SOFT_RESET

This request flushes all buffers and resets the Bulk Out and Bulk In pipes to their default states, and also resets all parallel port hardware and registers to their default state. This command is supported in all three alternate interface settings.

USB Port (continued)

Vendor-Specific Requests

Vendor-specific requests supported by the USS-720.

Table 17. Vendor-Specific Requests

Label	bmRequestType	bRequest	wValue	wIndex	wLength	Data
GET_1284_REGISTER	11000000B	3	Address	Zero	7	Register Data
SET_1284_REGISTER	01000000B	4	Address Data	Zero	Zero	[None]

GET_1284_REGISTER

The high byte of the wValue field specifies the address of the register that is to be read. The USS-720 responds by returning the current values in all of the parallel port registers. This command is only supported in interface 0, alternate setting 2. Attempts to issue this command to alternate settings 0 or 1 will result in a stall.

SET_1284_REGISTER

The wValue field specifies the address of the parallel port register to be written in the high byte and the value to be written in the low byte. This command is only supported in interface 0, alternate setting 2. Attempts to issue this command to alternate settings 0 or 1 will result in a stall.

IEEE 1284 Port

The *IEEE* 1284 port on the USS-720 is compliant with the *IEEE* 1284-1994 standard. The parallel port operates in two distinct modes. In fully Automatic Mode, the *IEEE* 1284 protocol is implemented completely in hardware. Compatibility Mode, Nibble Mode, and ECP Mode (with or without RLE compression) are supported, with all negotiation, termination, and other features of the protocol handled transparently by the hardware. The USS-720 also features a Register Mode, which presents a standard register interface to the host. These two modes provide the host with two distinct operating paradigms. In Automatic Mode, the host software interacts with the USS-720 as if with a USB-capable printer; while in Register Mode, the USS-720 emulates standard PC parallel port hardware. In the Automatic Mode, the host application software doesn't know that the USB data stream is being converted to *IEEE* 1284 protocol. In the Register Mode, it need not know that its interaction with parallel port registers is actually talking place remotely over a USB link.

Automatic mode is recommended for almost all applications. (**Note**: The drivers included in the Lucent Technologies USS-720 Evaluation Kit use only Automatic Mode.) Automatic Mode implements all negotiation handshakes automatically for Compatibility, Nibble, and ECP modes. In Register mode, the user must do the negotiations manually in software. Register mode can be useful when implementing a nonstandard parallel port interface.

Register-Based Operation

In its Register Mode of operation, the USS-720 emulates standard host-side parallel port hardware, with the register accesses being performed remotely over a USB connection. As in the standard register set, the interface mode is controlled by the Mode field in the Extended Control Register. The supported modes and their meanings are given in the Extended Control Register section on page 20, and operation and required software interaction for each of the supported modes are described in the sections that follow.

Standard Mode (000)

In this mode, the parallel port is under full software control, with no form of hardware assist. Software has complete control of all parallel port signals. This mode can be used for negotiations, terminations, proprietary handshake sequences, etc. As in standard host-side parallel port hardware, the parallel port data lines are unidirectional outputs in this mode.

Bidirectional Mode (001)

This mode is identical to Standard Mode (000), except that the direction of the parallel port data lines may be controlled with the Direction bit in the Control Register.

Compatibility Mode (010)

This mode provides hardware-based Compatibility Mode data transfers. Data sent to the USS-720 over the Bulk Out pipe will be transferred automatically to the peripheral using Compatibility Mode.

ECP Mode (011)

This mode provides hardware-based ECP Mode data transfers. To use ECP, the host software should negotiate for ECP Mode via the Control and Status Registers, then set Mode to 011. At this time, the Compress Enable bit in the USS-720 Control Register should also be set appropriately.

EPP Mode (100)

This mode provides hardware-based EPP Mode data transfers. To use EPP, the host software should negotiate for EPP Mode via the Control and Status Registers, and then set Mode to 100.

EPP mode in the USS-720 has the following data transfer rate characteristics. Note that the rates are approximate.

Table 18. Transfer Rates

Direction	UHCI	OHCI
Forward	1 Mbyte/s	1 Mbyte/s
Reverse	250 bytes/s	1 Kbyte/s

Because the reverse channel operation is implemented in the USB Control Pipe, the transfer rates are limited according to the particular implementation of the host controller, either UHCI or OHCI.

The high performance of the forward direction in EPP mode makes it attractive for implementations requiring little reverse channel traffic.

IEEE 1284 Port (continued)

Registers

Nine parallel port registers are available to the host. They are read and written using the GET_1284_REGISTER and SET_1284_REGISTER vendor-specific commands described above. The SET_1284_REGISTER writes a value into a particular register. Writes may either affect the configuration of the hardware or have a direct effect on parallel port control lines. In the case of the EPP Registers, writes initiate EPP write cycles on the parallel port.

The GET_1284_REGISTER returns seven register values: Status, Control, Extended Control, USS-720 Control, Data, EPP Address/Data, and USS-720 Setup Registers, in that order (see 19). Register values can also be read via the Interrupt pipe, which returns the values of Status, Control, Extended Control, and USS-720 Control Registers, in that order (see Table 20). Reads may affect the contents of the registers in one of two ways. Any register read clears any interrupt status that may exist at the time of the read. Also, a read targeting the EPP address or EPP Data Register will initiate the appropriate EPP read cycle on the parallel port. The value returned will be the address or data byte read from the peripheral as a result of that read cycle.

Table 19. GET_1284_REGISTER Data

Byte	Register Data
0	Status
1	Control
2	Extended Control
3	USS-720 Control
4	Data
5	EPP Address/Data
6	USS-720 Setup

Table 20. Interrupt Pipe Read Data

Byte	Register Data
0	Status
1	Control
2	Extended Control
3	USS-720 Control

Each of the nine registers are described in detail in Tables 21—29.

IEEE 1284 Port (continued)

Data Register

Table 21. Data Register

Data Register								Address: 0
Bit	7	6	5	4	3	2	1	0
Symbol	D7	D6	D5	D4	D3	D2	D1	D0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Description
7—0	D7—D0	**Data.** This register is equivalent to and operates in the same manner as the Data Register in a standard host-side parallel port controller chip. The register is writable when Auto Mode is 0 and the Mode field in the Extended Control Register is set to 000 or 001. It is always readable. The read value will be the value of the data latched into the register unless the Mode field is set to 001 and the Direction bit in the Control Register is set to 1 (Input Mode). In this case, the read value will be the value present on the parallel port data lines.

Status Register

Table 22. Status Register

Status Register								Address: 1
Bit	7	6	5	4	3	2	1	0
Symbol	nBusy	nAck	PError	Select	nFault	—	PLH	Timeout
Access	Read	Read	Read	Read	Read	Read	Read	Read
Default	X	X	X	X	X	X	X	0

Bit	Symbol	Bit Description
7	nBusy	**Inverted Busy.** An inverted version of the parallel port Busy signal.
6	nAck	**Parallel Port nAck Signal.**
5	PError	**Parallel Port PError Signal.**
4	Select	**Parallel Port Select Signal.**
3	nFault	**Parallel Port nFault Signal.**
2	—	**Reserved.**
1	PLH	**Peripheral Logic High.** The parallel port PLH signal.
0	Timeout	**EPP Time-Out.** This bit indicates that a time-out has occurred during an EPP read or write. If the peripheral fails to respond to an EPP read or write for longer than 10 µs, this bit will be set and an interrupt will be returned if interrupts are enabled. This bit is cleared by a read.

IEEE 1284 Port (continued)

Control Register

Table 23. Control Register

Control Register								Address: 2
Bit	7	6	5	4	3	2	1	0
Symbol	HLH	EPP mask	Direction	Int enbl	SelectIn	nInit	AutoFd	Strobe
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	0	0	1	1	0	0

Bit	Symbol	Bit Description
7	HLH	**Host Logic High.** The parallel port HLH signal.
6	EPP mask	**EPP Time-Out Interrupt Mask.** This bit masks the generation of an interrupt upon time-out of an EPP data or address transfer. Note that in typical host-side parallel port controller chips, this interrupt condition is grouped with and controlled by the Interrupt Enable bit in this register; so for exact emulation of typical parallel port hardware, this bit should always be written with the inverse of the Interrupt Enable bit.
5	Direction	**Parallel Port Direction.** When the Mode field in the Extended Control Register is set to 001, this bit controls the direction of the parallel port data lines. When set to 0, the lines are in Output Mode, and when set to 1, they are in Input Mode (see the Data Register on previous page). This bit also controls the direction of the interface in ECP Mode (011). It has no effect in Modes 000 or 010 (which are unidirectional only), or 100 (where the direction is uniquely determined by the type of access to the EPP Registers).
4	Int enbl	**Interrupt Enable.** This bit enables interrupt generation on nAck events. If this bit is set, interrupt status will be generated on transitions of nAck from low to high (this status being reflected by the nAck Interrupt bit in the USS-720 Control Register).
3	SelectIn	**Inverted nSelectIn.** An inverted version of the parallel port nSelectIn signal.
2	nInit	**Parallel Port nInit Signal.**
1	AutoFd	**Inverted nAutoFd.** An inverted version of the parallel port nAutoFd signal.
0	Strobe	**Inverted nStrobe.** An inverted version of the parallel port nStrobe signal.

IEEE 1284 Port (continued)

EPP Address Register

Table 24. EPP Address Register

EPP Address Register								Address: 3
Bit	7	6	5	4	3	2	1	0
Symbol	A7	A6	A5	A4	A3	A2	A1	A0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Description
7—0	A7—A0	**EPP Address.** This register is equivalent to and operates in the same manner as the EPP Address Register in a standard host-side parallel port controller chip. The register is writable when Auto Mode is 0 and the Mode field in the Extended Control Register is set to 100. A write to this register initiates an EPP address write transfer on the parallel port. The register is always readable. When the Mode is set to 100, a read access will initiate an EPP address read transfer on the parallel port, and the value returned will be the address value read from the peripheral. Reads when not in Mode 100 will return whatever value has been previously latched, but will not have any effect on the parallel port.

EPP Data Register

Table 25. EPP Data Register

EPP Data Register								Address: 4
Bit	7	6	5	4	3	2	1	0
Symbol	D7	D6	D5	D4	D3	D2	D1	D0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Description
7—0	D7—D0	**EPP Data.** This register is equivalent to and operates in the same manner as the EPP Data Register in a standard host-side parallel port controller chip. The register is writable when Auto Mode is 0 and the Mode field in the Extended Control Register is set to 100. A write to this register initiates an EPP data write transfer on the parallel port. The register is always readable. When the Mode is set to 100, a read access will initiate an EPP data read transfer on the parallel port, and the value returned will be the data value read from the peripheral. Reads, when not in Mode 100, will return whatever value has been previously latched, but will not have any effect on the parallel port.

IEEE 1284 Port (continued)

ECP Command Register

Table 26. ECP Command Register

ECP Command Register								Address: 5
Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Access	Write	Write	Write	Write	Write	Write	Write	Write
Default	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Description
7—0	C7—C0	**ECP Command.** This register is equivalent to the ECP Address FIFO Register in a standard host-side parallel port controller chip, but has some different restrictions on its usage. The register is writable when Auto Mode is 0 and the Mode field in the Extended Control Register is set to 011 and there is no ECP data in either the Bulk Out buffers or in the process of being transmitted. Writes to this address in a mode other than 011 will be ignored; writes while in mode 011 and when the hardware is busy will generate a NAK. The value written to this register will be transferred to the peripheral as an ECP command.

IEEE 1284 Port (continued)

Extended Control Register

Table 27. Extended Control Register

Extended Control Register								Address: 6
Bit	7	6	5	4	3	2	1	0
Symbol	Mode[2]	Mode[1]	Mode[0]	nAck interrupt	nFault interrupt	Bulk In interrupt	Bulk In empty	Bulk Out empty
Access	R/W	R/W	R/W	Read	Read	Read	Read	Read
Default	0	0	0	0	0	0	1	1

Bit	Symbol	Bit Description
7—5	Mode[2:0]	**Mode.** In Register Mode (when Auto Mode is 0), this bit controls the mode of the parallel port interface. This field is equivalent to the Mode field in a standard host-side parallel port controller chip. The supported modes are as follows: **Mode[2:0] Mode Description** 000 Standard Mode Full software control, data lines are output only 001 Bidirectional Mode Full software control, data lines are bidirectional 010 Compatibility Mode Hardware handshaking 011 ECP Mode Software negotiations, hardware data transfers 100 EPP Mode Software negotiations, hardware data transfers 101 Reserved 110 Reserved 111 Reserved For more information, see the Register-Based Operation section on page 14.
4	nAck Interrupt	**nAck Interrupt.** This bit will be set when the parallel port nAck signal makes a transition from 0 to 1 while the Interrupt Enable bit in the Control Register is set to 1. Interrupt status is cleared by any register read.
3	nFault Interrupt	**nFault Interrupt.** This bit will be set when the parallel port nFault signal makes a transition from 1 to 0 while the nFault Interrupt Mask bit in the USS-720 Control Register is set to 0. An interrupt will also be generated if the mask bit goes low while nFault is low. Interrupt status is cleared by any register read.
2	Bulk In Interrupt	**Bulk In Interrupt.** This bit will be set when Bulk In data is available and the Bulk In Interrupt Mask bit in the Control Register is set to 0. This allows software to use the interrupt pipe to automatically receive notification of available Bulk In data rather than polling with Bulk In requests. Interrupt status is cleared by any register read.
1	Bulk In Empty	**Bulk In Empty.** This bit will be clear when there is Bulk In data available for reading by the host, and set when there is not.
0	Bulk Out Empty	**Bulk Out Empty.** This bit will be clear when there is Bulk Out data waiting in the buffers or in the process of being transmitted over the parallel port, and set otherwise.

IEEE 1284 Port (continued)

USS-720 Control Register

Table 28. USS-720 Control Register

USS-720 Control Register								Address: 7
Bit	7	6	5	4	3	2	1	0
Symbol	Discon. int mask	Change int mask	Bulk In int mask	Bulk Out int mask	nFault int mask	Reserved	Compress enable	Auto mode
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	0	1	1

Bit	Symbol	Bit Description
7	Discon. int mask	**Disconnect Interrupt Mask.** This bit masks the generation of an interrupt on the detection of what appears to be a disconnection of the peripheral from the parallel port. Disconnect is detected when the Peripheral Logic High signal changes from 1 to 0, or when all parallel port lines driven by the peripheral are high for a long period of time.
6	Change int mask	**Change Interrupt Mask.** This bit masks the generation of an interrupt on the detection of a transition on any of the parallel port lines driven by the peripheral.
5	Bulk In int mask	**Bulk In Interrupt Mask.** This bit masks the generation of an interrupt when Bulk In data is available for reading by the host.
4	Bulk Out int mask	**Bulk Out Interrupt Mask.** This bit masks the generation of an interrupt when the Bulk Out data path goes empty.
3	nFault int mask	**nFault Interrupt Mask.** This bit masks the generation of an interrupt falling edge of nFault when Mode is set to 011 (ECP Mode).
2	Reserved	**Reserved.** This bit must always be written to 0.
1	Compress enable	**Compress Enable.** This bit enables automatic hardware-based RLE compression of outgoing data, for use in ECP with RLE Mode. If software desires to use this feature, this bit should be set before attempting to send data. This bit **must** be cleared for proper operation in ECP (without RLE) Mode.
0	Auto mode	**Auto Mode.** Setting this bit puts the chip in fully Automatic Mode. When set, USS-720 can handle all communications with the peripheral with no assistance from software, and all registers except the USS-720 Control Register are read only. Clearing this bit enables write access to the other registers and disables all automatic operation, provided that none has yet taken place.

IEEE 1284 Port (continued)

USS-720 Setup Register

Table 29. USS-720 Setup Register

USS-720 Setup Register								Address: 8
Bit	7	6	5	4	3	2	1	0
Symbol	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Filter Software Override	Filter Enable
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Description
7	Reserved	**Reserved.**
6	Reserved	**Reserved.**
5	Reserved	**Reserved.**
4	Reserved	**Reserved.**
3	Reserved	**Reserved.**
2	Reserved	**Reserved.**
1	Filter Software Override	**Filter Software Override.** When this bit is set, software can control the digital filtering of incoming parallel port signals with the Filter Enable bit. When clear, filters are controlled by the pull-up or pull-down stage of the SUSPEND pin. (See Filter Bypass Mode.)
0	Filter Enable	**Filter Enable.** Controls digital filtering of incoming parallel port signals when the Filter Software override bit is set. Setting to 1 enables filtering; clearing this bit disables filtering.

IEEE 1284 Port (continued)

Interrupts

The USS-720 can return interrupt status on the interrupt pipe. Interrupt status may be generated as a result of one of seven separately maskable conditions. Any interrupts that are pending will no longer be pending after a read operation. The individual conditions are described in the sections that follow.

nAck Interrupt

The nAck interrupt is enabled by setting the Interrupt Enable bit in the Control Register. An interrupt will be generated whenever nAck transitions from 0 to 1. Interrupt status is indicated by the nAck Interrupt bit in the Extended Control Register.

EPP Time-Out Interrupt

The EPP time-out interrupt is enabled by setting the EPP Time-Out Interrupt Mask bit in the Control Register to 0. Note that this is a change from typical host-side parallel port hardware, where interrupts on EPP time-out conditions are enabled by the Interrupt Enable bit in the Control Register.

An EPP time-out occurs when the peripheral fails to respond to an EPP handshake within the time allowed by the *IEEE* 1284 specification. If this occurs, there is no reliable way to determine whether the peripheral is still functioning or not, or whether the byte in transit was transferred properly, and it will be up to software to attempt to recover by resetting the connection or some other means.

nFault Interrupt

The nFault interrupt is enabled by setting the nFault Interrupt Mask bit in the USS-720 Control Register to 0. Interrupt status is reported via the nFault Interrupt bit in the Extended Control Register. The interrupt is generated when in ECP Mode and either the nFault line transitions from 1 to 0 or the nFault line is low and the interrupt is unmasked. This may indicate that the peripheral has reverse data to transmit.

Bulk In Interrupt

The Bulk In interrupt is enabled by setting the Bulk In Interrupt Mask bit in the USS-720 Control Register to 0. Interrupt status is reported by the Bulk In Interrupt bit in the Extended Control Register, as well as the Bulk In Empty bit in the same register. This interrupt is generated when there is Bulk In data available for reading by the host. By enabling this interrupt, the host may use the automatic polling of the interrupt pipe to receive notification of incoming data, rather than explicitly polling the Bulk In pipe.

Bulk Out Interrupt

The Bulk Out interrupt is enabled by setting the Bulk Out Interrupt Mask bit in the USS-720 Control Register to 0. Bulk Out empty status is reported via the Bulk Out Empty bit in the Extended Control Register. This interrupt is generated when the Bulk Out data pipeline goes completely empty. By enabling this interrupt, the host may use the automatic polling of the interrupt pipe to be notified of the completion of a data transfer, rather than explicitly polling the Bulk Out Empty bit.

Change Interrupt

The Change interrupt is enabled by setting the Change Interrupt Mask bit in the USS-720 Control Register to 0. There is no Interrupt Status bit associated with the Change Interrupt. This interrupt is generated when any of the parallel port signal lines driven by the peripheral (nAck, Busy, nFault, PError, Select, or PLH) change state.

Disconnect Interrupt

The Disconnect interrupt is enabled by setting the Disconnect Interrupt Mask bit in the USS-720 Control Register to 0. There is no Interrupt Status bit associated with the Disconnect interrupt. This interrupt is generated when the Peripheral Logic High signal makes a transition from 1 to 0, or when Peripheral Logic High is 0 and all other parallel port signal lines driven by the peripheral (nAck, Busy, nFault, PError, and Select) are high for longer than one second. Either of these conditions should indicate that the peripheral has been disconnected from the USS-720.

External Circuitry Requirements

The USS-720 is intended to be a single-chip solution. As such, the USB transceiver and the *IEEE* 1284 buffers have been integrated on-chip. External requirements include a 3.3 V supply and a 1.5 kΩ ± 5% pull-up resistor for the DPLS pin. If the internal oscillator is used, a 12 MHz crystal along with bias capacitors are needed (see Figure 3). If the internal oscillator is not used, a 12 MHz clock signal should be supplied to CLK_LO, and CLK_HI should be left unconnected. 1.2 kΩ ± 5% pull-up resistors are needed on all *IEEE* 1284 signals (except PLH), unless used in the High Drive Mode (see the following page). A 5 V supply and USB and/or *IEEE* 1284 connectors might also be needed, depending on the application.

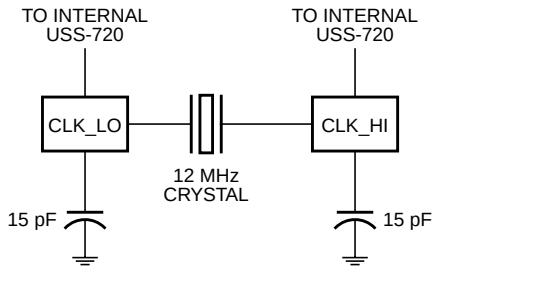


Figure 3. External Crystal Connection

Figure 4 shows the normal USS-720 connection to the USB. Both DPLS and DMNS require 24 Ω ± 1% series resistors for USB impedance matching. Additionally, a 1.5 kΩ pull-up resistor is required on DPLS for full-speed/low-speed differentiation.

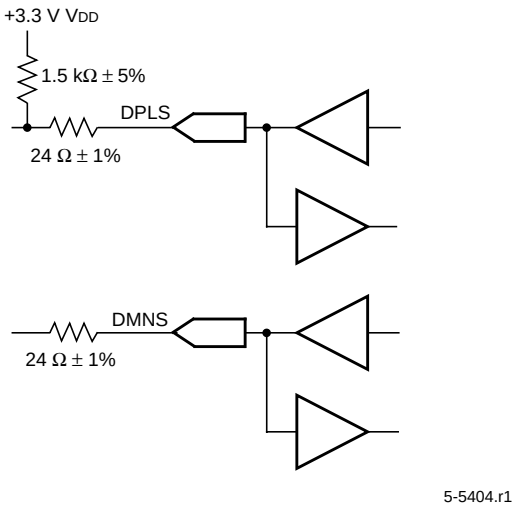


Figure 4. USB Transceiver Connection (Normal Mode)

For using the USS-720 in a self-powered device, there are some additional considerations. The device must refrain from supplying power through the pull-up resistor when the device is plugged into an unpowered bus. The USS-720 device circuit must also ensure that the DPLS and DMNS lines are in an appropriate state when the device is powered but not plugged in. Figure 5 shows an example connection to meet these requirements.

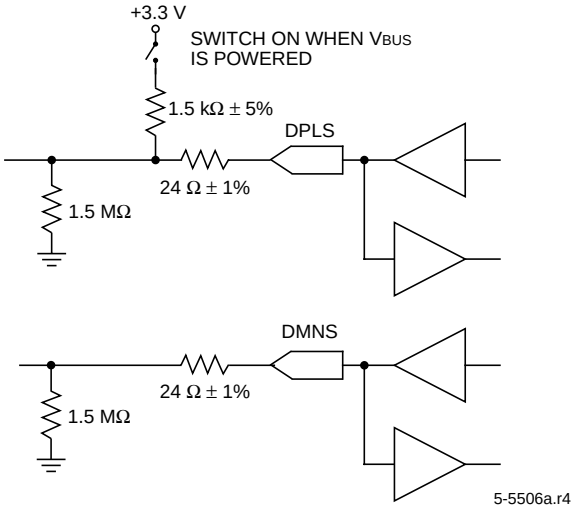


Figure 5. Self-Powered Device Example Connection

Figure 6 shows a USS-720-to-*IEEE* 1284 parallel port connection that complies with the *IEEE* 1284 specification. Other connections are also possible. While the *IEEE* specification requires these resistors, developers must make their own design decision against the 500 µA suspend mode current requirements required by the USB specification.

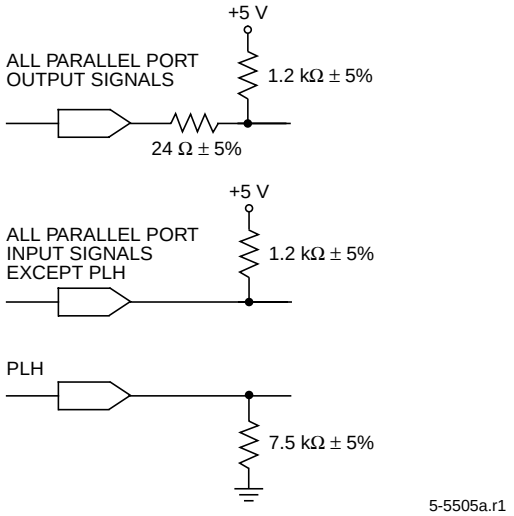


Figure 6. USS-720 Connection to *IEEE* 1284

Filter Bypass Mode

For embedded applications, the USS-720 *IEEE* 1284 port can be operated in Filter Bypass Mode. This mode disables digital filtering of the parallel port signals into the USS-720, providing a performance improvement.

Note: Since digital filtering is disabled, the parallel port lines will be susceptible to noise. Do **not** use this mode when driving across a cable.

Filter Bypass Mode is enabled by connecting a 20 kΩ pull-down resistor to the SUSPEND line.

High Drive Mode

If desired (e.g., for embedded applications), the USS-720 *IEEE* 1284 port can operate in High Drive Mode. In this mode, all parallel port signals are constantly driven by 14 mA totem-pole drivers, rather than with the normal open-drain drivers. This eliminates the need for external pull-up resistors on the parallel port signals (and, if driving another chip on the same board, there is no need for the 24 Ω impedance matching resistors). High Drive Mode is enabled by connecting a 20 kΩ pull-down resistor to the SK line.

Self-Powered Mode

When using the USS-720 in a self-powered application, attach a 5 kΩ pull-up resistor to the CS line. This causes the correct self-powered status to be reported in response to a USB Get-Status command.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 30. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature Range	T_A	0	70	°C
Storage Temperature	T_{stg}	–40	125	°C
Voltage on Any Pin with Respect to Ground	V_{IN}	V_{SS} – 0.3	V_{DD} + 0.3*	V

* Except for 5 V tolerant buffers where V_{IN} max = V_{DD5} max + 0.3 V. V_{IN} must never exceed V_{DD5} + 0.3 V at any time. V_{DD5} should be selected to satisfy this condition.

Electrical Characteristics

Table 31. dc Characteristics (T_A = 0 °C to 70 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage:						
Low	V_{IL}	—	—	—	0.8	V
High	V_{IH}	—	2.0	—	—	V
Output Voltage:						
Low	V_{OL}	—	—	—	0.4	V
High	V_{OH}	—	2.4	—	—	V
Power Dissipation	P_D	25 °C, V_{DD} = 3.3 V	1.65	231	323.4	mW
Power Supply Voltage	V_{DD}, V_{DDA}	—	3	3.3	3.6	V
	V_{DD5}	5 V environment	4.375	5	5.5	V
		3 V environment	3	3.3	3.6	V
Power Supply Current	I_{DD}	—	0.5	70	98	mA

Table 32. USB Transceiver Driver Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Rise and Fall Times:		OEN = 0, C_L = 50 pF			
(10%—90%)	t_R		4	20	ns
(90%—10%)	t_F		4	20	ns
Rise/Fall Time Matching	t_{RFM}	OEN = 0, C_L = 50 pF	90	110	%
Crossover Point	V_{CRS}	OEN = 0, C_L = 50 pF	1.3	2.0	V
Output Impedance	Z_{DRV}	OEN = 0	28	43	Ω

The USS-720 is a 3.3 V part, and it has separate pins ($V_{DD}5$) for power to the *IEEE* 1284 drivers. Capacitance values for the USS-720 pins are listed in Table 33.

Table 33. Capacitance Values

Parameter	Value	Unit
CLK_LO	1.0	pF
CLK_HI	1.0	pF
All Other Pins	3.0	pF

Timing Characteristics

- Timing is specified over the operating range from 0 °C to 70 °C ambient temperature, V_{DD} = 3.0 V to 3.6 V, and $V_{DD}5$ = 4.75 V to 5.25 V.
- All timing is referenced from the rising edge of CLK_LO, with 70 pF output load.
- Only DIO is required to meet these input setup and hold times for proper operation. For other inputs, meeting the limit is only required to ensure that the signal will be recognized on the referenced clock edge rather than one period later.

Table 34. Setup and Hold Input Timing

Parameter	Setup Time	Hold Time	Unit
DIO Setup and Hold	2.9	3.4	ns

Table 35. Clock Characteristics/Miscellaneous Input Timing

Parameter	Symbol	Min	Typical	Max	Unit
Frequency of Operation (CLK_LO)	f	11.976	12.000	12.024	MHz
Clock Period	tcyc	83.1	83.3	83.5	ns
Duty Cycle	—	—	40/60*	—	%

* The duty cycle applies to any frequency in the specified range.

Table 36. Output Delay Timing

Parameter	Min	Max	Unit
PDATA Output Delay	5.3	21.5	ns
NUSB_RESET Output Delay	6.5	17.1	ns
SUSPEND Output Delay	2.6	34.6	ns
SK Output Delay	6.4	16.0	ns
CS Output Delay	—	75.0	ns
DIO Output Delay	3.6	31.6	ns

Table 37. Miscellaneous Output Timing

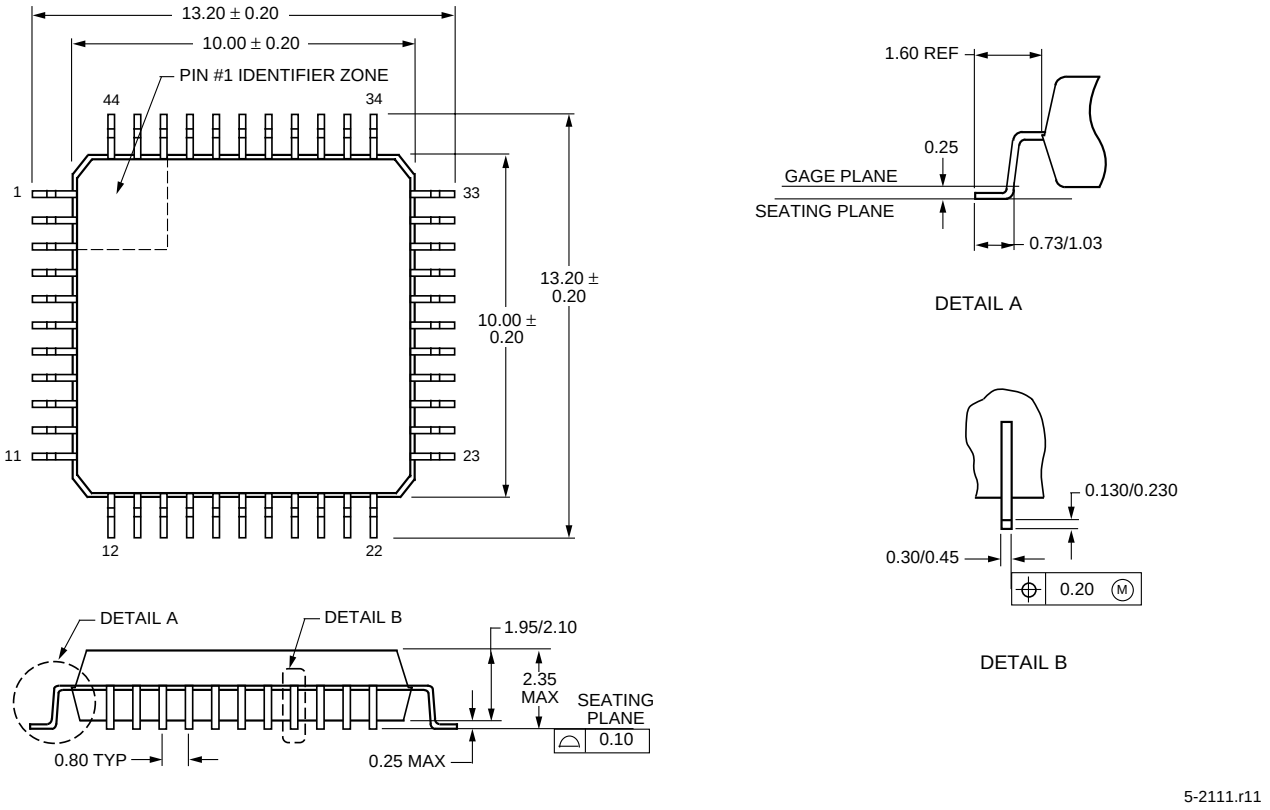
Parameter	Symbol	Min	Typical	Max	Unit
Frequency of Operation (SK)	f	390	429	476	kHz
Clock Period	tcyc	2.10	2.33	2.56	µs
Duty Cycle	—	—	50/50*	—	%

* The duty cycle applies to any frequency in the specified range.

Outline Diagram

44-Pin MQFP

Dimensions are in millimeters.



5-2111.r11

Ordering Information

Device Code	Package	Comcode
USS720F-DB	44-Pin MQFP	108271057

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